Listing of Claims:

Please cancel all claims and insert the following new claims:

1 (New) An apparatus, comprising:

a memory buffer including

a memory module sub-interface to communicate with one or more memory modules,

a chipset sub-interface to communicate with a chipset, the chipset sub-interface being electrically isolated from the memory module sub-interface,

a data latch to latch data being transferred between the chipset sub-interface and the memory module sub-interface such that the chipset sub-interface and memory module sub-interface operate independently but in synchronization with each other, and

control logic to coordinate an output of data from the memory buffer in an interleaved mode with data from another memory buffer.

2 (New) The apparatus of claim 1, wherein the chipset sub-interface includes outputs to be interleaved.

3 (New) The apparatus of claim 1, wherein the control logic is to coordinate an output of data in a wired-OR interleaved mode.

4 (New) The apparatus of claim 1, wherein the control logic is to coordinate the output of the data interleaved with data from a single other memory buffer.

5 (New) The apparatus of claim 1, wherein the memory buffer further comprises a voltage supply line to receive a supply voltage that is independent of an operating voltage of the chipset.

6 (New) The apparatus of claim 1, wherein the memory buffer further comprises:

a first voltage supply line to receive a first supply voltage that is compatible with an operating voltage of the chipset; and

a second voltage supply line to receive a second

supply voltage that is compatible with an operating voltage of the memory modules.

7 (New) The apparatus of claim 1, wherein:

the memory module sub-interface includes a first number of data lines to communicate with the memory modules; and

the chipset sub-interface includes a second number of data lines to communicate with the chipset, the second number being different than the first number.

8 (New) The apparatus of claim 7, wherein the first number is twice the second number.

9 (New) The apparatus of claim 1, wherein the memory module sub-interface comprises fixed length stub data lines to communicate with the memory modules.

10 (New) The apparatus of claim 1, wherein:

the memory module sub-interface is to operate at a first voltage; and

the chipset sub-interface is to operate at a

second voltage, the second voltage being different than the first voltage.

11 (New) The apparatus of claim 10, wherein the first voltage is between 1.2 and 1.8 volts.

12 (New) The apparatus of claim 10, wherein the second voltage is less than 1.0 volt.

13 (New) The apparatus of claim 1, wherein:

the memory module sub-interface is to operate at a first frequency; and

the chipset sub-interface is to operate at a second frequency, the second frequency being different than the first frequency.

14 (New) The apparatus of claim 13, wherein the first frequency is greater than the second frequency.

15 (New) The apparatus of claim 1, wherein the memory module sub-interface comprises a dynamic random access memory (DRAM) sub-interface to communicate with a DRAM module.

16 (New) The apparatus of claim 1, wherein the memory module sub-interface comprises a double data rate (DDR) DRAM sub-interface to communicate with a DDR DRAM module.

17 (New) The apparatus of claim 1, wherein the memory module sub-interface comprises a double data rate quad data rate (QDR) DRAM sub-interface to communicate with a QDR DRAM module.

18 (New) The apparatus of claim 1, further comprising:

a second memory buffer including

a second memory module sub-interface to communicate with one or more memory modules, and

a second chipset sub-interface to communicate with the chipset, the second chipset sub-interface being electrically isolated from the second memory module sub-interface, the second chipset sub-interface including outputs to output data in an interleaved mode with data from the memory buffer.

19 (New) An apparatus, comprising:

a memory buffer including

a memory module sub-interface to communicate with a memory module,

a chipset sub-interface to communicate with a chipset, the chipset sub-interface being electrically isolated from the memory module sub-interface and including outputs to output data in an interleaved mode with data from another memory buffer, and

a data latch to latch data being transferred between the chipset sub-interface and the memory module sub-interface such that the chipset sub-interface and memory module sub-interface operate independently but in synchronization with each other.

20 (New) The apparatus of claim 19, wherein the chipset sub-interface comprises outputs to be interleaved in a wired-OR configuration.

21 (New) An apparatus comprising:

a buffer to be disposed in an interface between a chipset and one or more memory modules, the buffer including

a first sub-interface with one of the

chipset and the memory modules,

a second sub-interface with the other of the chipset and the memory modules, the second sub-interface operated at a different voltage level and at a lower frequency than the first sub-interface, and

control logic to coordinate an output of data from the buffer in an interleaved mode with data from another buffer.

22 (New) The apparatus of claim 21, further comprising:

a second buffer to be disposed in the interface between the chipset and one or more memory modules, the second buffer including a second set of data outputs, the second set of data outputs being interleaved with outputs from one of the first sub-interface and the second sub-interface to form the multiple interleaved interface outputs.

23 (New) The apparatus of claim 21, wherein:

the first sub-interface comprises a sub-interface with the chipset; and

the multiple interleaved buffer outputs are to

output data over the first sub-interface to the chipset.

24 (New) The apparatus of claim 21, wherein:

an operating voltage level of said first sub-interface is less than 1.0 volt; and

an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

25 (New) The apparatus of claim 21, wherein the first sub-interface is operated at twice the frequency of the second sub-interface.

26 (New) The apparatus of claim 21, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.